고성능 AIPS 내의 연산증폭기에 대하여 부저항소자를 사용한 이득개선방법

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요 약

고성능 VLSI 아날로그 정보처리시스템(AIPS)에서 고이득 Op-Amp는 기본적 정보처리소자이다. 증폭기는 시스템내 피드백루프에 사용시 안정도와 정확도를 얻기 위하여 고이득이 요구된다. 1단의 증폭으로 이득이 충분하지 않을 경우 이득 부스팅 또는 추가적인 이득단이 필요하다. 본 논문에서 부저항소자를 사용할 경우 이득이 개선되며 1단으로 고이득을 손쉽게 얻을 수 있음을 보였다. 기존의 방법에 비교하여 본 연구에 제안된 방법은 전출력 스윙, 적은 회로면적과 전력소비, 그리고 여러 구조의 증폭기에 적용가능하다는 잇점을 지니고 있다. 부저항소자는 Op-Amp에 사용될 경우 (+)와 (-) 차동출력 사이에 설치되어 증폭기 출력저항을 상쇄한다. 부저항소자를 교차연결된 CMOS 인버터의 형태로 구현할 경우 간단한 구조로서 40 dB 보다 더 큰 이득개선을 손쉽게 얻을 수 있음을 HSPICE 시뮬레이션을 통하여 확인하였다.

키워드 : 연산증폭기, 이득개선회로, 부저항소자

A Gain Enhancing Scheme for Op-Amp in High Performance AIPS Using Negative Resistance Element

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ABSTRACT

In the high performance Analog Information Processing Systems(AIPS), gain boosting or additional gain stage is required when the gain is not sufficient with one stage amplification. This work shows that high gain is neatly obtained by enhancing the gain using the negative resistance element. Compared to the conventional techniques, the proposed scheme enjoys full output swing, small circuit area and power consumption, and the applications to various configurations of amplifiers. The negative resistance element is placed between the differential output nodes when used in the Op-Amp. The HSPICE simulation indicates that enhancement of more than 40 dB is readily obtained in this simple configuration when the negative resistance element is implemented in the form of cross-coupled CMOS inverters.

Key Words : Op-Amp, Gain Enhancement Circuit, Negative Resistance Element

1. Introduction

In the state of the art VLSI Analog Information Processing Systems(AIPS), high gain Op-Amp is the basic processing element. High gain is needed to provide stability and accuracy when the Op-Amp stage is placed in the feedback loop. However, when the gain is not sufficient with one stage, gain boosting is required if additional amplifying stages are not allowed. Gain boosting was achieved in complicated ways before, by placing regulator amplifiers in the feedback loop[1, 2] or by using replica amplifiers[3-5]. Techniques utilizing positive feedback are also in use[6, 7].

These ideas all suffer from the limited output swing[1, 2], increased circuit area and power consumption[3-5] and the limited usage only to fully differential amplifiers[6, 7]. This paper shows that these difficulties can be overcome and the gain can be greatly enhanced by using a simple negative resistance element. When this element is connected in parallel with the output resistance of the amplifier, the overall output resistance increases due to the compensating role of the negative resistance element. This element can be readily implemented taking on the form of cross-coupled CMOS inverters.

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2. The gain enhancing scheme

(Fig. 1) shows the basic scheme for the gain enhancing circuit. Here, an amplifier with output resistance R_o is connected in parallel with the external negative resistance element $-R_e$. G_m is the transconductance of the amplifier.

Since the element is put in parallel with the output resistance of the original amplifier, the DC gain of the amplifier becomes

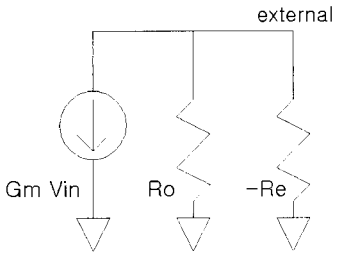
$$A_v = G_m \cdot [R_o \| (-R_e)] \quad (1)$$

$$= G_m \cdot \frac{R_o(-R_e)}{(R_o - R_e)} \quad (2)$$

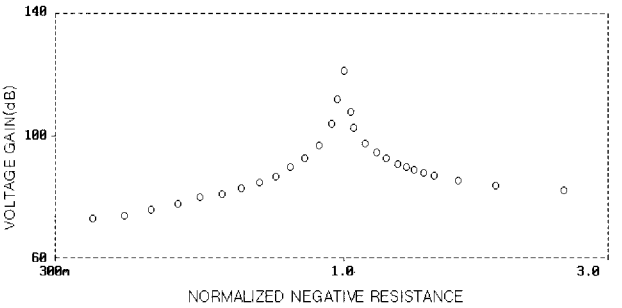
Consider a very large negative resistance, larger than R_o. From eq.2, the gain is positive and the value is close to DC case. As one moves the negative resistance toward a smaller value, it approaches R_o and the denominator of eq.2 becomes small. The negative resistance begins to compensate R_o and the gain increases. When R_e becomes equal to R_o, the gain becomes infinite in principle. As R_e passes R_o, the denominator becomes large and the gain begins to decrease. This time, the gain becomes negative and there occurs the 180 degree phase reversal. When R_e becomes much less than R_o, the gain becomes $|A_v|=G_mR_e$.

(Fig. 2) shows the variation of the DC gain of an Op-Amp in terms of negative resistance. The variation is shown as a function of normalized negative resistance, i.e., R_e/R_{ex}. R_{ex} is the value of the negative resistance of the element when there is the exact match between the output resistance of the amplifier and the negative resistance of the element. This is the value of the negative resistance giving the peak gain. Note that there is a sharp increase of gain exceeding 120dB at $R_e/R_{e,max}=1$. Note also that when the negative resistance is large, the gain equals that of the original amplifier, but when it becomes small, the gain equals that approximately G_mR_e.

To implement the negative resistance element, consider an inverting amplifier of any type with the transconductance $G_{m,inv}$ and the output resistance $R_{o,inv}$. The inverter is normally biased at the switching threshold $V_{dd}/2$. Then consider a cross-coupled inverter pair. The signal circulating inside the pair is equivalent to the one propagating through a long chain of inverters. When the inverters are driven in a positive feedback and $G_{m,inv}$ wins over $R_{o,inv}$, the circuit forms the negative resistance element[8]. In this case, when one places a voltage source having internal resistance between the output nodes of the pair, the internal resistance is reduced and the voltage difference at the output nodes of the inverters is amplified. This is the way the element can be utilized for the enhancement of the gain of amplifiers.



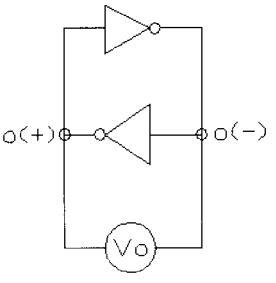
(Fig. 1) The basic configuration for the gain enhancing circuit



(Fig. 2) The gain enhancement in terms of Re/Re,max

3. The negative resistance element

In principle, any type of inverting amplifier can be employed to implement the negative resistance. For the fully differential amplifiers, for instance, one may employ the negative resistance element with cross-coupled inverters as shown in (Fig. 3) This element is usually employed in VLSI circuits to speed up the node with large parasitic resistance[8]. Lately negative resistance is used in the LC-tank Voltage Controlled Oscillators(VCO) currently in wide use for mobile telecommunications to compensate the losses in the LC-tank[9]. This element can be readily inserted into the fully differential amplifier circuit with the output nodes o(+) and o(-) providing the inputs of the cross-coupled inverters.



(Fig. 3) The negative resistance element

As far as the scheme is concerned, it does not discern any sort of inverting amplifiers. Therefore, regular CMOS, NMOS, and even bipolar amplifiers can be employed for the scheme. For the discussions to follow, we focus on the CMOS inverting amplifier, whose negative resistance is easily matched to the output resistance of the original amplifier by choosing adequate W/L ratio for n and p-devices.

4. Application of proposed scheme to the operational amplifiers

4.1 Two-stage operational amplifier

One may test the proposed scheme for any type of amplifying circuit. For instance, the usual fully differential Op-Amps, such as folded cascode, telescopic amplifiers can be good examples to test the scheme. These amplifiers will be discussed later. Here as the first example, an Op-Amp test circuit is taken from[10] as shown in (Fig. 4) This is the class A/AB 2-stage fully differential amplifier employed for low voltage operation.

The gain enhancement in this amplifier can be implemented in several ways. The first one is to enhance the output resistance of the first stage. The second one is to enhance the second stage. The last one is to enhance both stages. The first one can be achieved by inserting the negative resistance element between the drain of input p-transistors. The second one can be done by inserting the element between the differential output of the amplifier o(+) and o(-) The third one can be done by combining the above two configurations.

The open loop DC gain of this amplifier is written as

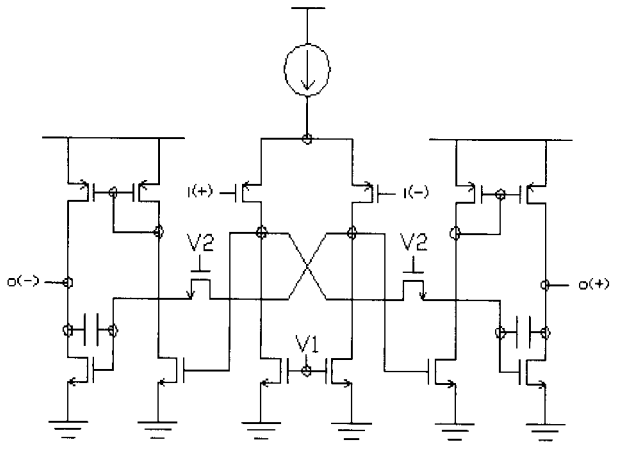
$$A_v = A_{v1} \cdot A_{v2} \tag{3}$$

$$\cong [g_{mi1p}(r_{o1n} \| r_{o1p})] \cdot [(g_{mi2n} + g_{mi2p})(r_{o2n} \| r_{o2p})] \tag{4}$$

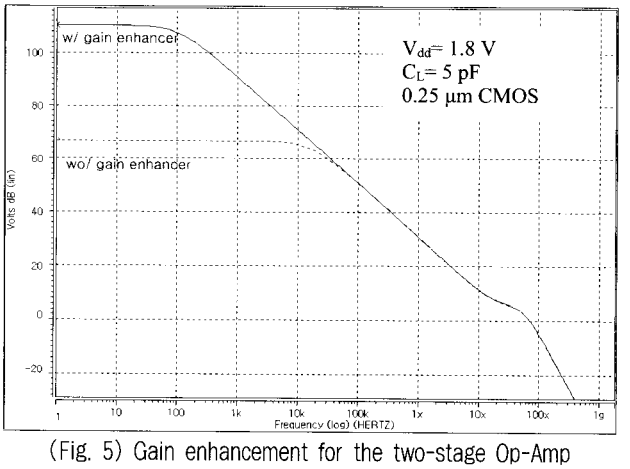
Here g_{mi1p} and g_{mi2n}, g_{mi2p} are the transconductances of input p-transistor of the first stage and input n and p-transistors of the second stage respectively. r_{o1n}, r_{o1p} and r_{o2n}, r_{o2p} are the output resistances of n and p-transistors for each stage. The output resistance of each stage, $(r_{o1n}||r_{o1p})$ and $(r_{o2n}||r_{o2p})$, can then be compensated by employing the adequate negative resistance element. The gain can be further enhanced by using two elements for both the first and the second stages.

The initial design of the amplifier gives the open loop DC gain of 66 dB. To enhance the gain, the negative resistance element was inserted for the second stage i.e., between the differential outputs o(+) and o(-) of the amplifier. After employing the negative resistance element, the gain increases to 110 dB. This is shown in (Fig. 5) The dotted gain is the one without gain enhancer and the solid gain is with the gain enhancer. This is from the HSPICE simulation. The load capacitance C_L is 5 pF. Employed V_{dd} is 1.8 V for the following discussions. The gain could be further enhanced by compensating the output resistances of both stages by employing two negative elements. When the first stage is also enhanced, the gain increased to 150 dB.

A semi-qualitative guideline can be presented as follows to estimate the size of the inverter transistors in the negative resistance element. Consider the compensation at the output nodes of the second stage for instance. The output resistance $(r_{o2n}||r_{o2p})$ needs to be canceled by a negative resistance $-R_e$. Then $R_e=(r_{o2n}||r_{o2p})$ should hold. For the inverter in the negative resistance element, the following condition should be satisfied when the negative resistance action occurs and cancels the output resistance exactly[8]:



(Fig. 4) The two-stage Op-Amp



(Fig. 5) Gain enhancement for the two-stage Op-Amp

$$(g_{mn}+g_{mp})R_e > 4 \tag{5}$$

Therefore the minimum required transconductance is written

$$g_{mn}+g_{mp}=\frac{4}{R_e}=\frac{4}{(r_{o2n}\,\|\,r_{o2p})} \tag{6}$$

The inverter transistors are in saturation during the negative resistance operation. Utilizing $g_m=\sqrt{2(W/L)\mu C_{ox}I_D}$, the required aspect ratios of inverter transistors can be obtained from the following relation:

$$\left[\sqrt{2(W/L)_n\mu_n C_{ox}I_{Dn}}+\sqrt{2(W/L)_p\mu_p C_{ox}I_{Dp}}\right]=\frac{4}{(r_{o2n}\,\|\,r_{o2p})} \tag{7}$$

I_{Dn} and I_{Dp} are the bias currents of n and p-transistors. In case one allocates equal portion of transconductance to the n and p-transistors, i.e., $g_{mn}=g_{mp}$, $(W/L)_n$ becomes

$$\left(\frac{W}{L}\right)_n=\frac{1}{2\mu_n C_{ox}I_{Dn}}\left[\frac{2}{(r_{o2n}\,\|\,r_{o2p})}\right]^2 \tag{8}$$

Then based on the assumption $g_{mn}=g_{mp}$, $(W/L)_p$ can be found correspondingly from the following relation:

$$\frac{(W/L)_p}{(W/L)_n}=\frac{\mu_n I_{Dn}}{\mu_p I_{Dp}} \tag{9}$$

Eq.8 presents an important insight regarding the applicability of the proposed scheme. When $(r_{o2n}\|r_{o2p})$ is high, the RHS of eq.8 becomes small and the W/L ratio is low for the n and p-transistors. The channel length L should be taken large correspondingly. This is not a problem for the 2-stage amplifier when the output resistance of each stage is moderate, and the output resistance can be canceled with adequate W/L ratio. However, this may not be the case for the cascode (folded or telescopic) amplifiers having high output resistance. The output resistance is $g_m r_o$ times higher in these amplifiers compared to the uncascoded amplifiers. To compensate such output resistance, extremely large L may be required. In this case, one should utilize the output resistance of uncascoded transistors for the compensation rather than the output transistors. This point will be discussed further in the next section for the cascode Op-Amp.

The cross-coupled negative resistance element can be employed for any sort of amplifier configuration. For instance, this element can be also used for the single ended amplifiers as well as the fully differential amplifiers. For this purpose, the element is used for the input differential stage, and compensates the output resistance of the stage. This will be shown later for the low cost simple Op-Amp.

4.2 Cascode Op-Amps

For the cascode amplifiers, there is an important consideration to note: as the device is closer to the output, the output resistance is larger due to cascoding, and the channel length of the canceling inverter is unreasonably large as eq.8 indicates. These cascoded devices cannot be utilized for the scheme that cancels with negative resistance. Rather the devices useful for the gain enhancement are the ones closer to the supplies, i.e., the uncascoded devices and if one applies the scheme to these devices, the Op-Amp with maximum gain can be designed with reasonable channel lengths. This will be discussed for a folded-cascode Op-Amp shown in (Fig. 6).

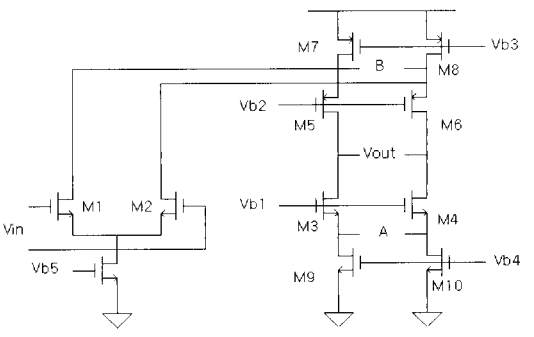
The DC gain of folded-cascode Op-Amp is given as

$$A_v=g_{m1}\{[(g_{m5}+g_{mb5})r_{o5}(r_{o1}\,\|\,r_{o7})]\,\|\,[(g_{m3}+g_{mb3})r_{o3}r_{o9}]\} \tag{10}$$

$$=g_{m1}\cdot\frac{(g_{m5}+g_{mb5})r_{o5}(r_{o1}\,\|\,r_{o7})(g_{m3}+g_{mb3})r_{o3}r_{o9}}{(g_{m5}+g_{mb5})r_{o5}(r_{o1}\,\|\,r_{o7})+(g_{m3}+g_{mb3})r_{o3}r_{o9}} \tag{11}$$

$$=g_{m1}\cdot\frac{(g_{m5}+g_{mb5})(g_{m3}+g_{mb3})}{(g_{m5}+g_{mb5})\cdot\dfrac{1}{r_{o3}r_{o9}}+(g_{m3}+g_{mb3})\cdot\dfrac{1}{r_{o5}(r_{o1}\,\|\,r_{o7})}} \tag{12}$$

This gain is maximized when enhanced by reducing the denominator of eq.12 to 0. There can be 3 cases for implementing this. The first two cases are compensating r_{o9} with negative resistance $-R_A=-\dfrac{(g_{m5}+g_{mb5})r_{o5}(r_{o1}\,\|\,r_{o7})}{(g_{m3}+g_{mb3})\cdot r_{o3}}$ and compensating r_{o7} with $-R_B=-\dfrac{(g_{m3}+g_{mb3})r_{o1}r_{o3}r_{o9}}{(g_{m5}+g_{mb5})r_{o1}r_{o5}+(g_{m3}+g_{mb3})r_{o3}r_{o9}}$.



(Fig. 6) Folded-cascode Op-Amp

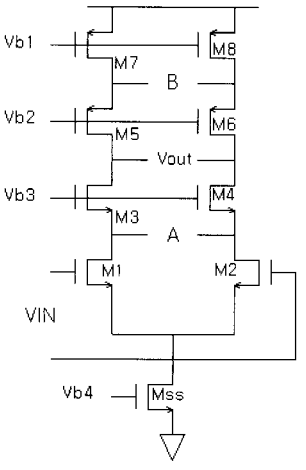
To implement this scheme, one takes the following strategy: For the first case for instance, (1) connect the negative resistance element $-R_e$ in parallel with r_{o9}, thereby making the total output resistance negative and (2) equate $(-R_e \| r_{o9})$ to $-R_A$. Increase of gain exceeding 40 dB is obtained for the first two cases by this method. The third case corresponds, from eq.12, to increasing r_{o3} and r_{o5} indefinitely and is not handled with the negative resistance element technique.

Note that the first two cases imply the negative resistance elements should be placed at the proper nodes, other than the output node, to make the channel length for the inverters in the negative resistance inverter reasonably small. For this reason, the negative resistance element is not placed at the output node but placed between the drain of transistors M9 and M10 (A) or M7 and M8 (B) in (Fig. 6). This corresponds to the first two cases involving uncascoded output resistance r_{o7} and r_{o9} which can be handeled with moderate W/L ratio of negative resistance inverter.

This consideration is also the case with the telescopic amplifier. This amplifier is shown in (Fig. 7). The small signal gain of the amplifier is given as

$$A_v = g_{m1}[(g_{m3}r_{o3}r_{o1}) \| (g_{m5}r_{o5}r_{o7})] \tag{13}$$

$$= g_{m1} \cdot \frac{g_{m3}g_{m5}r_{o1}r_{o3}r_{o5}r_{o7}}{g_{m3}r_{o1}r_{o3} + g_{m5}r_{o5}r_{o7}} \tag{14}$$



(Fig. 7) Telescopic Op-Amp

The denominator can be made 0 by compensating r_{o1}, r_{o3}, r_{o7}, r_{o5} with the values $-\frac{g_{m5}r_{o5}r_{o7}}{g_{m3}r_{o3}}$, $-\frac{g_{m5}r_{o5}r_{o7}}{g_{m3}r_{o1}}$, $-\frac{g_{m3}r_{o1}r_{o3}}{g_{m5}r_{o5}}$, $-\frac{g_{m3}r_{o1}r_{o3}}{g_{m5}r_{o7}}$ respectively, in a similar fashion for the folded cascade amplifier. Among these, the first or the third setting can be employed since in the cascoded configuration, the output resistance r_{o3} or r_{o5} of the output transistors M_3 and M_5 cannot be isolated. Instead the cascoded resistance $(g_{m1}r_{o1})$ r_{o3} and $(g_{m7}r_{o7})$ r_{o5} appear at the output and should be canceled. As discussed previously, this requires very large channel length for the canceling inverter. Therefore one should seek to utilize the uncascoded transistor with moderate W/L ratio to enhance the gain of the amplifier. For instance, when the element is placed at the drains of bottom n-devices M1 and M2(A), the simulation indicates the gain is enhanced from 61 dB to 129 dB. When the element is used at the drains of top p-devices M7 and M8(B), the gain increases to 109 dB.

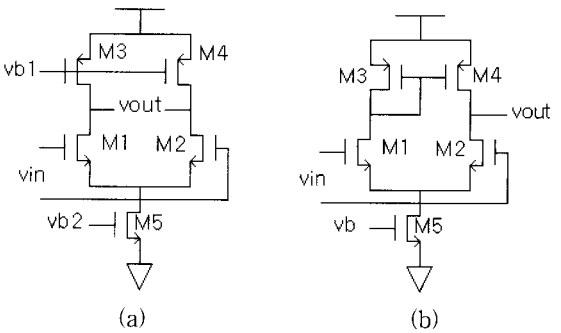
4.3 Simple differential amplifier as an Op-Amp

Using the technique of output resistance cancellation by negative resistance, it is noted that the simple differential amplifier can be transformed into a high gain Op-Amp. This is an important point and is the key advantage of the proposed method. For this purpose, one may employ the usual simple differential amplifiers as in (Fig. 8).

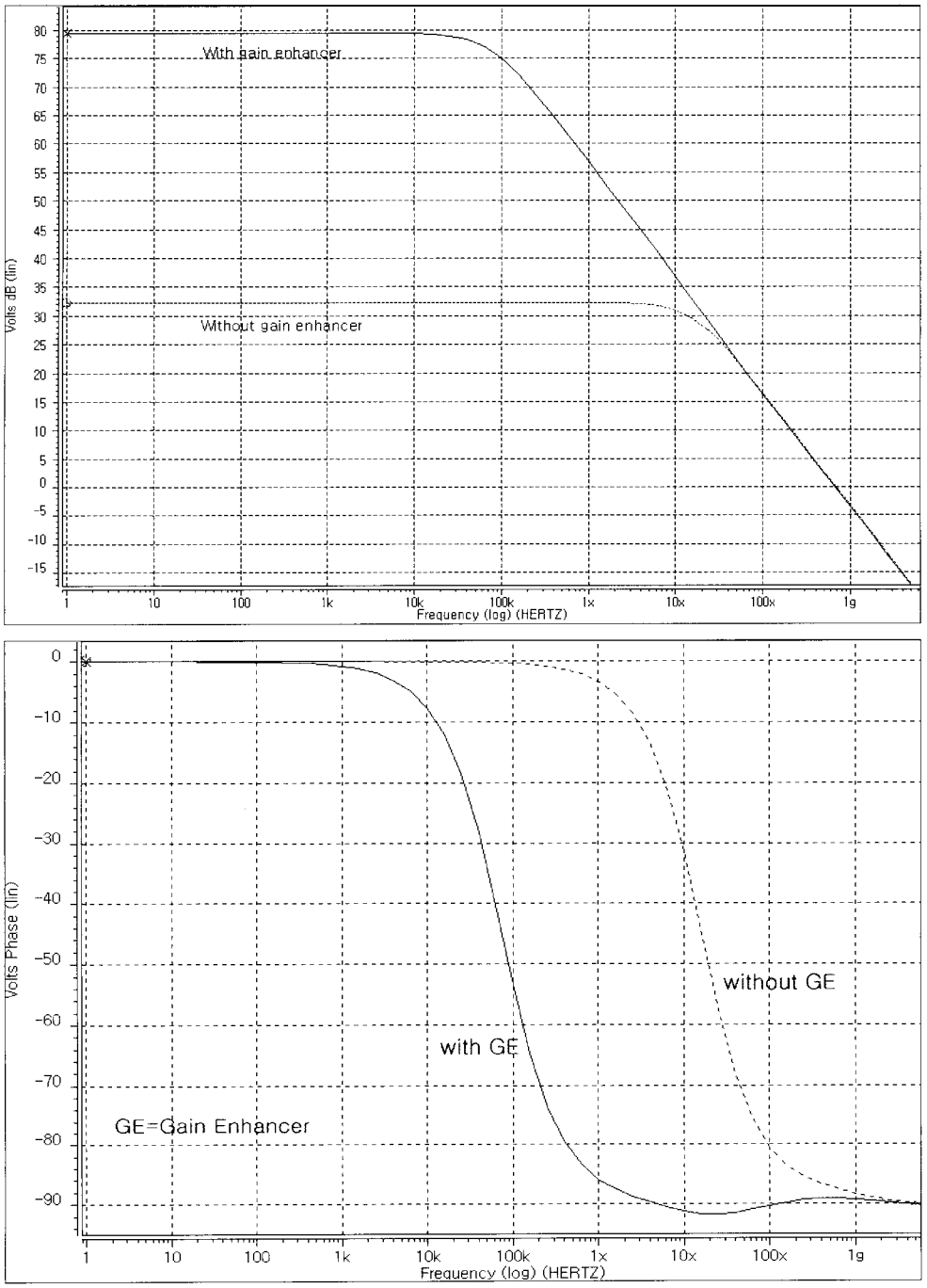
Consider the amplifier (a) The gain of the amplifier is given as

$$A_v = -\frac{g_{m1}}{g_{d1} + g_{d3}} \tag{15}$$

Initially this amplifier has the differential gain of 32dB by design. The denominator is canceled using a negative resistance element. After canceling the output resistance, the gain increases to 80dB. This is shown in (Fig. 9). Dotted curve is the gain of the unenhanced amplifier and the solid curve is that of the enhanced amplifier. This indicates that the simple differential amplifier can work as an economical low cost high gain Op-Amp. The phases



(Fig. 8) Simple amplifiers (a) fully differential (b) single ended



(Fig. 9) Gain and phase of the differential amplifiers

are also shown. It is noted that the phase deterioration is negligible(only 1 degree) at the unity gain frequency 670 MHz due to gain enhancement. This implies the stability is sustained when the proposed scheme is employed for the Op-Amp.

The scheme of increasing differential gain by canceling the output resistance with negative resistance element can apply also to the single ended configuration of the amplifier shown in (Fig. 8)(b) This time, the negative resistance inverters are connected between the output of the amplifier and the drain of M3 which is diode connected. In this case, typical simulation indicates that the unenhanced gain of 40dB increases to 121dB when the scheme is used.

The proposed negative resistance scheme of this paper enjoys several advantages over the previous works[1-7]. The regulator amplifier technique[1, 2] is basically equivalent to the cascode configuration and therefore suffers from the voltage headroom issue at the output. Having no extra device along the output signal path, the proposed

scheme does not have this problem. The replica amplifier technique[3, 4] duplicates the amplifier circuit, therefore doubling the circuit area and power consumption. For the N-transistor amplifier, the total number of transistor required in this method is 2N. Meanwhile the number of transistor in the proposed scheme is N+4. Power consumption due to the negative resistance digital inverters is negligible, less than 5% of total power in most cases. The method suggested in [6, 7] obtains positive feedback by cross-connecting the active load p-devices symmetrically. Therefore this method applies to the symmetric fully differential amplifiers only. However, the proposed scheme in this paper is based on the cancelation of the output resistance of the stage, thus applying virtually to all types of Op-Amps., i.e., to the single and multi-stage amplifiers and also to the asymmetric single ended amplifiers as well as to the symmetric fully differential amplifiers. This can be cited as the most important advantage of the proposed scheme.

For the wide-band amplifiers, the proposed scheme has also a significant advantage. For the wide-band amplifiers, the gain is correspondingly lower and it would be very beneficial if there exists a scheme which may improve the gain without sacrificing the bandwidth. In this respect, the proposed scheme is attractive especially for the wide-bandwidth operational amplifiers. One designs for the wide-bandwidth amplifier and then enhances the differential gain by inserting a couple of inverters without reducing the bandwidth.

The gain enhancement for the simple differential amplifier proposed in this paper is compared with previous work in <Table 1>.

Note that if the inverters in the element are biased close to the common mode of the Op-Amp at half the V_{dd}, there can be short circuit overlap currents and DC power consumption due to negative resistance element exists. However, the extra-power the negative resistance element carries would not be a significant problem and can be minimized since, due to the asymmetric transfer characteristic of the inverters in the element, the realistic location of the switching points is considerably off the common mode level of the Op-Amp at exact $V_{dd}/2$ where the DC power consumption is nominally maximum. Therefore the extra-power can be kept at the minimum level and is typically on the order of only 10% of the total power consumed by the Op-Amp alone.

<Table 1> Comparison with previous work

	Reference [6]	This work
Gain after enhancement	84dB	80dB
Gain before enhancement	68dB	32dB
Gain Enhancement Ratio	1.23	2.5
Single ended config.	No	Yes
Phase margin	59deg.	91deg.
Power consumption	14.4mW	0.94mW
Supply voltage	1.8V	1.8V
Technology	0.21um CMOS	0.25um CMOS

5. Conclusion

The discussion in this paper showed that the gain of Op-Amps can be enhanced by using the negative resistance element. The negative resistance element is implemented with cross-coupled CMOS inverters. When this element is connected in parallel with the output resistance of the amplifier, the overall output resistance increases due to the compensating role of the negative resistance element. When adequately designed, this element provides sufficient additional gain exceeding 40dB. While enjoying minimal penalties in circuit area and power consumption, this scheme does not introduce additional poles and does not deteriorate high frequency settling behavior. Therefore this scheme can be a viable alternative to the conventional techniques such as regulator amplifier in feedback loop or replica amplifiers.

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