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Gate Sizing Of Multiple-paths Circuit

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ABSTRACT

Logical Effort [1, 2] is a simple hand-calculated method that measures quick delay estimation. It has the advantage of reducing the design cycle time. However, it has shortcomings in designing a path for minimum area or power under a fixed-delay constraint. The method of overcoming the shortcomings is shown in [3], but it is constrained for a single logical path.

This paper presents an advanced gate sizing method in multiple logical paths based on the equal delay model. According to the results of the simulation, the power dissipation for both the existing logical effort method and proposed method is almost equal. However, compared with the existing logical effort method, it is about 52 (%) more efficient in space.

Keywords : Logical Effort, Optimizing Power-Delay, Equal Delay Model, Gate Sizing

다중 논리경로 회로의 게이트 크기 결정 방법

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요 약

논리 노력[1, 2]의 기법은 회로의 지연 값을 간단한 필산으로 신속하게 측정할 수 있는 기술이다. 이 기법은 설계 공정 시간을 절약하는 장점도 있지만 고정 지연이라는 조건에서 논리 경로의 면적이나 전력 소비를 최소화하여 설계할 수 없는 단점이 있다. 이 단점을 보완하는 방법을 논문[3]에서 제안하였지만, 논리 경로가 하나인 회로에만 국한되어 적용할 수 있는 방법이었다.

본 논문에서는, 균형 지연 모델을 기초로, 다중 논리 경로의 회로에 적용할 수 있는 향상된 게이트 크기 결정 방법을 제한하고자 한다. 시뮬레이션 결과, 기존 논리노력 방법과 비교하면 전력 소비 측면에서 거의 같았지만 회로의 설계 공간 측면에서는 약 52%의 효율성을 보였다.

키워드 : 논리 노력, 전력-지연 최적화, 균등 지연 모델, 게이트 크기 결정

1. Introduction

The method of the logical effort [1, 2] is an easy way to estimate the delay in a CMOS circuit. The simplicity and clarity of the logical effort model have allowed many studies to accurately adapt the model to different design conditions. For example, reference [4] introduces an extension of the logical effort model that considers the I/O coupling capacitance and the input ramp effect, and a simple model that calculates transistor sizes of an asynchronous control circuits with circular paths is shown in [5]. The logical effort extension model that considers temperature and voltage variation is also introduced in [6] and its application to FPGA interconnect driver sizing is well discussed in [7].

The logical effort model has shortcomings in designing a path for minimum area or power under a fixed-delay constraint [2]. It is proposed to overcome the above shortcomings by optimizing energy-delay efficiency using the equal delay model in [3]. However, their results were achieved by handling the gate sizing problem in a single logical path. In comparison, this paper presents an advanced gate sizing method in multiple logical paths with multiple fan-outs in series based on the equal delay model.

This paper is presented in the following. Chapter 2 introduces the equal delay model proposed in [3]. Gate sizing problems in multiple paths are discussed and their solution is proposed based on the equal delay model in

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chapter 3. In particular gate sizing method is extended for the general circuits with multiple fan-outs in series in chapter 4. In chapter 5, through the example of two different circuits, we compare the logical effort with our proposed technique to obtain the simulation results using Hspice. We summarize and conclude our proposed technique in chapter 6.

2. Overview of logical effort and equal delay model

The logical effort assumes an equal effort delay per stage of the circuit while our equal delay model assumes an equal delay per stage.

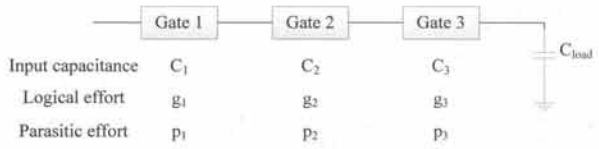

Fig. 1. A three-stage logical path

Fig. 1 shows the circuit driving a load on the logical path, which is composed of 3 stages. Each gate is characterized by four parameters: delay (d), logical effort (g), electrical effort (h) and parasitic effort (p). The effort delay (f) of the logic gate is the product of between logical effort and electrical effort. We assume that there is no delay and load between signal lines connecting gates. D is defined as a delay needed for driving load (C_{load}) in the logical path where input capacitance is limited to a certain value.

In this paper we choose the minimum-sized inverter with a P-to-N ratio of 2 as the standard inverter. We also express the delay of each element in terms of (τ) and capacitance in units of (k), the input capacitance of a standard inverter as shown in [5].

If the delay per stage in the logical path is the same, each stage's delay is given as $d_1 = d_2 = d_3 = D/3$. Thus, we can establish the following equations on the basis of the overall delay, logical effort, electrical effort and parasitic effort in the above three-stage logical path.

$$d_1 = \frac{D}{3} = f_1 + p_1 = g_1 h_1 + p_1 \tag{1}$$

$$d_2 = \frac{D}{3} = f_2 + p_2 = g_2 h_2 + p_2 \tag{2}$$

$$d_3 = \frac{D}{3} = f_3 + p_3 = g_3 h_3 + p_3 \tag{3}$$

In the case of no branch, the input capacitance of the next stage is the load of the currently processing stage. So, we can substitute h_1, h_2, and h_3 with C_2/C_1 , C_3/C_2 , and C_{load}/C_3, respectively. This delivers the following equations.

$$d_1 = \frac{D}{3} = \frac{g_1 * C_2}{C_1} + p_1 \tag{4}$$

$$d_2 = \frac{D}{3} = \frac{g_2 * C_3}{C_2} + p_2 \tag{5}$$

$$d_3 = \frac{D}{3} = \frac{g_3 * C_{load}}{C_3} + p_3 \tag{6}$$

With the above equations arranged with respect to the input capacitance, respectively, the following equations are derived.

$$C_1 = \frac{g_1 * C_2}{\left(\frac{D}{3} - p_1\right)} = \frac{g_1 * g_2 * g_3 * C_{load}}{\left(\frac{D}{3} - p_1\right)\left(\frac{D}{3} - p_2\right)\left(\frac{D}{3} - p_3\right)} \tag{7}$$

$$C_2 = \frac{g_2 * C_3}{\left(\frac{D}{3} - p_2\right)} = \frac{g_2 * g_3 * C_{load}}{\left(\frac{D}{3} - p_2\right)\left(\frac{D}{3} - p_3\right)} \tag{8}$$

$$C_3 = \frac{g_3 * C_{load}}{\left(\frac{D}{3} - p_3\right)} \tag{9}$$

With expansion of these equations for n-stage circuits, the input capacitance of i-th stage is derived as in the following equation.

$$C_i = C_{load} \prod_{k=i}^{n} \frac{g_k}{\left(\frac{D}{n} - p_k\right)} \tag{10}$$

This equation is directly applied to compute input capacitance in a logical path with stage number and C_{load}, and is analogous to the capacitance transformation equation for logical effort model [2], which is used to compute input capacitance backward starting at the end of the logical path.

Here, the value of D/n should be larger than the largest parasitic effort value. Because the input capacitance of the first stage C_1 is the input capacitance in the logical path, it must satisfy the constraint condition of input capacitance in the logical path.

3. The method of gate sizing in multiple paths of being only one fan-out.

3.1 Multiple paths gate sizing based on equal delay model

Fig. 2 shows a logic circuit with two paths. Path 1 drives C_{load1} through C_{11} and C_{12} while path 2 drives C_{load2} through C_{21}. Assume that path 1 is the longest and thus, is a critical path with delay D under the given delay constraint.

The previous paper [3] showed that, for optimal power dissipation, gate sizing should be made for the total delay of a single path to be close to the maximum delay constraint in a logical path. This paper will also show that, even in multiple paths, the total power dissipation of path 1 and path 2 can be optimized with gate sizing under the total delay of path 1 and path 2 to be close to the given delay constraint in a logical path.

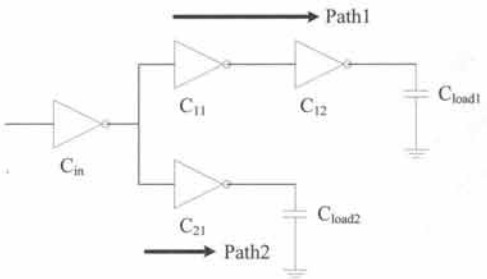

Fig. 2. A logic circuit with paths

Let delay of each stage along path 1 be equally distributed as in the following equation.

$$D = d_{C_{in}} + d_{C_{11}} + d_{C_{12}} \tag{11}$$

With applying equal delay model to path 1,

$$d_{C_{in}} = d_{C_{11}} = d_{C_{12}} = \frac{D}{3} \tag{12}$$

However, this circuit is composed of multiple paths (two paths) and C_{in} drives both C_{11} and C_{21}. Therefore, it is not guaranteed that the delay of C_{in} stage equal to that of C_{11} stage driving C_{12} or that of C_{12} stage driving C_{load1}. If the delay of C_{in} stage is x times that of C_{11} stage or that of C_{12} stage, then

$$d_{C_{in}} = xd_{C_{11}} = xd_{C_{12}} \tag{13}$$

If we denote the delay of C_{11} stage or C_{12} stage as d_1 (delay of path 1), then

$$d_{C_{in}} = xd_{C_{11}} = xd_{C_{12}} = xd_1 \tag{14}$$

In path 2, if we assume that the delay of C_{in} stage is y times that of C_{21} stage and denote the delay of C_{21} stage as $d2$, then

$$d_{C_{in}} = yd_{C_{21}} = yd_2 \tag{15}$$

With equal delay model applied to the circuit of Fig. 2. The basic equation that models the delay through a single logic gate, in units of (τ): $D=g*h+p$ where g is logical effort, h is electrical effort, and p is parasitic delay.

Path 1:

$$xd_1 = g_{C_{in}}\frac{(C_{11}+C_{21})}{C_{in}} + p_{C_{in}} \tag{16}$$

$$d_1 = g_{C_{11}}\frac{C_{12}}{C_{11}} + p_{C_{11}} \tag{17}$$

$$d_1 = g_{C_{12}}\frac{C_{load1}}{C_{12}} + p_{C_{12}} \tag{18}$$

Path 2:

$$yd_2 = g_{C_{in}}\frac{(C_{11}+C_{21})}{C_{in}} + p_{C_{in}} \tag{19}$$

$$d_2 = g_{C_{21}}\frac{C_{load2}}{C_{21}} + p_{C_{21}} \tag{20}$$

The logical effort is defined so that an inverter has a logical effort of 1 and a typical value of P_{inv}, the parasitic delay of an inverter is 1.

The above equations can be rearranged with respect to C as in the following equations.

Path 1:

$$C_{in} = \frac{C_{11}+C_{21}}{xd_1 - 1} \tag{21}$$

$$C_{11} = \frac{C_{12}}{d_1 - 1} \tag{22}$$

$$C_{12} = \frac{C_{load1}}{d_1 - 1} \tag{23}$$

Path 2:

$$C_{21} = \frac{C_{load2}}{d_2 - 1} \tag{24}$$

$$C_{in} = \frac{C_{11}+C_{21}}{yd_2 - 1} \tag{25}$$

In path1, $D = xd_1+d_1+d_1$. This leads to $d_1=D/(x+2)$.

In path2, $D = yd_2+d_2$. In (14) and (15) , $xd_1=yd_2$. Therefore,

Path 1:

$$d_1 = \frac{D}{x+2} \tag{26}$$

Path 2:

$$d_2 = D - xd_1 \tag{27}$$

For the given D value and the arbitrary x value, we can determine gate size along the logical paths using the above (21-27).

Table 1 shows gate size and total gate size for arbitrary x value, under the constraint of delay (=15 (τ)) and $C_{load1} = C_{load2} = 64$ (k).

Fig. 3 shows the C_{in} value and Fig. 4 shows the sum of total capacitance corresponding to x value, respectively.

From the results in both Fig. 3 and Fig. 4, C_{in} becomes the minimum at $x = 1.40$ while the sum of total capacitance becomes the minimum at $x = 0.40$.

Therefore, for the gate sizing for minimizing the total power dissipation, we have to find the x value which meets the sum of total capacitance at the minimum, under the constraint of input capacitance.

Table 1. Gate size corresponding to arbitrary x value

x value	0.20	0.30	0.40	0.50	0.60	1.00
C11	1.89	2.10	2.32	2.56	2.81	4.00
C12	11.0	11.6	12.2	12.8	13.4	16.0
C21	5.06	5.31	5.57	5.82	6.07	7.11
Cin	19.1	7.75	5.26	4.19	3.61	2.78
Sum	37.1	26.8	25.4	25.4	25.9	29.9
x value	1.20	1.40	1.50	2.00	3.00	4.00
C11	4.71	5.50	5.93	8.46	16.0	28.4
C12	17.4	18.8	19.5	23.3	32.0	42.7
C21	7.64	8.18	8.45	9.85	12.8	16.0
Cin	2.67	2.64	2.65	2.82	3.60	4.94
Sum	32.4	35.1	36.5	44.4	64.4	92.0

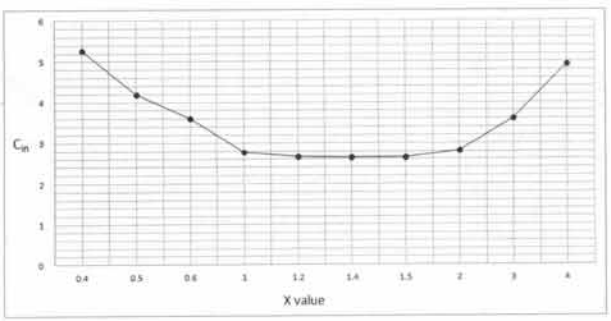

Fig. 3. C_{in} corresponding to arbitrary x value

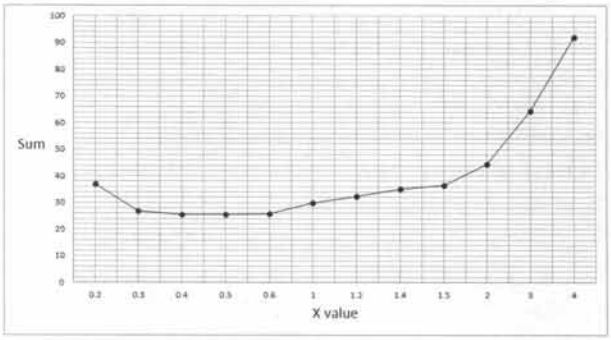

Fig. 4. Sum of total capacitances corresponding to arbitrary x value

If the constraint of input capacitance is 3.00 (k) $\leq C_{in} \leq 5.00$ (k), we can gate size to dissipate the minimum power with x value between 0.40 and 0.50. In addition, if the constraint of input capacitance is 2.60 (k) $\leq C_{in} \leq 2.70$ (k), we can gate size to dissipate the minimum power with x value between 1.00 and 1.20.

3.2 Formalization of gate sizing for multiple paths based on equal delay model

Fig. 5 shows a circuit that is composed of n-multiple paths and each path is composed of m_k - stages loading C_{loadk}.

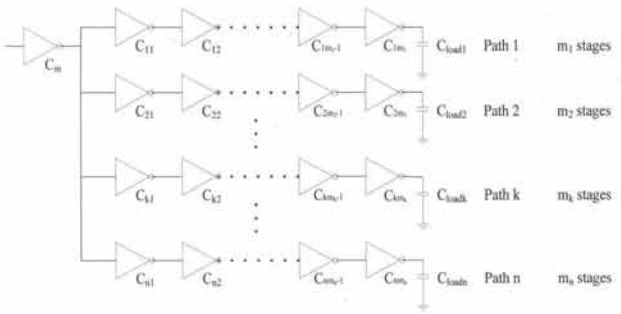

Fig. 5. n-multiple paths and each has m_k-stages along the logical path

Let $m_{critical}$ - stages denote a number of stages in a critical path and each stage have an equal delay of $d_{critical}$. C_{in} stage drives n-multiple paths and thus, the delay of it can be different from of $d_{critical}$. Therefore, in a critical path, the delay of C_{in} can be expressed as $xd_{critical}$.

The following equation can be derived in a critical path.

$$D = (x + m_{critical})d_{critical} \tag{28}$$

This equation can be rearranged with respect to dcritical and thus,

$$d_{critical} = \frac{D}{x + m_{critical}} \tag{29}$$

When the i-th stage inverter drives (i+1)-th stage inverter in the random path k, if we apply equal delay model to the path, then equation (30) is derived in the following.

$$d_k = \frac{C_{km_{i+1}}}{C_{km_i}} + 1 \tag{30}$$

The equation (31) can be derived by rearranging the above equation with respect to the i-th stage capacitance.

$$C_{km_i} = \frac{C_{km_{i+1}}}{d_k - 1} \tag{31}$$

In (31), $C_{kmi+1} = C_{loadk}$ if $m_i = m_k$.

The total power dissipation can be minimized if we set the delay in random path k to be equal to the delay in a critical path. Therefore, the equation (32) can be derived which states the relation of the total delay in random path k and equal delay in each stage.

$$D = xd_{critical} + m_k d_k \tag{32}$$

This equation can be rearranged with respect to d_k.

$$d_k = \frac{D - xd_{critical}}{m_k} \tag{33}$$

The substitution of (29) into (33) results in (34).

$$d_k = \frac{m_{critical} D}{m_k (x + m_{critical})} \tag{34}$$

The equation (35) can be obtained by applying equal delay model to C_{in} stage.

$$xd_{critical} = \frac{\sum_{i=1}^{n} C_{i1}}{C_{in}} + 1 \tag{35}$$

This equation can be arranged with respect to C_{in} and thus,

$$C_{in} = \frac{\sum_{i=1}^{n} C_{i1}}{xd_{critical} - 1} \tag{36}$$

3.3 Algorithm

Under a constraint delay value D and a constraint input capacitance value and a given random x value, the next algorithm will determine the gate sizing for the minimum power dissipation in the circuit with multiple paths.

Algorithm 1

```
//Mx - Set of random x values
//MCin - Set of constraint input capacitance values
//old temp - the minimum sum of total capacitances

initialization temp= 0, old temp=∞
for all x ∈ Mx do
   for every paths do
      Calculate delays in all paths by (29), (34)
      for every stages do
         Calculate all capacitance values by (31)
      end for
   end for
   Calculate of input capacitance value by (36)
   if Cin ∈ MCin then
      for every paths do
         for every stages do
            temp = sum of total capacitances
         end for
      end for
   end if
   if temp < old temp then
      old temp = temp
   end if
end for
```

4. The method of gate sizing in the multiple paths with multiple fan-outs in series.

Fig. 6 shows that the circuit is composed of seven inverters and two fan-outs.

Path 1 is assumed to be a critical path in the circuit and to have its delay D. The delay of each path should be "maximum delay D" to determine the gate sizing for the minimum power consumption. Let's assume that the delay of C_{in} is x_1 times the delay of C_{11} and the delay of C_{11} is x_2 times the delay of C_{12}.

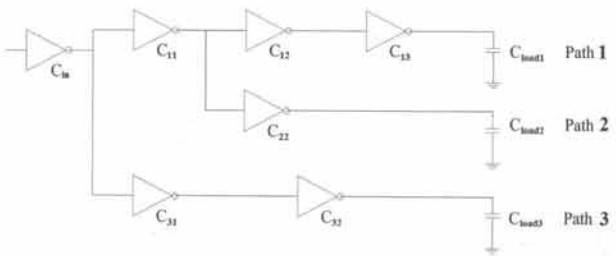

Fig. 6. The circuit composed of seven inverters and two fan-outs

Then, the following two equations can be derived from the above assumptions.

$$d_{C_{in}} = x_1 d_{C_{11}} \tag{37}$$

$$d_{C_{11}} = x_2 d_{C_{12}} \tag{38}$$

With the equal delay model applied to the above equations, the total delay of path 1 becomes $D = d_{C_{in}} + d_{C_{11}} + d_{C_{12}} + d_{C_{13}}$. If we assume $d_{C_{12}} = d_{C_{13}} = d_1$, the delay of path 1 becomes $D = (x_1 x_2 + x_2 + 2)d_1$. This equation can be rearranged with respect to d_1 as:

$$d_1 = \frac{D}{x_1 x_2 + x_2 + 2} \tag{39}$$

With the equal delay model applied to path 1, the following equations are derived for each stage.

$$d_{C_{in}} = x_1 x_2 d_1 = g_{C_{in}} \frac{C_{11} + C_{31}}{C_{in}} + p_{C_{in}} \tag{40}$$

$$d_{C_{11}} = x_2 d_1 = g_{C_{11}} \frac{C_{12} + C_{22}}{C_{11}} + p_{C_{11}} \tag{41}$$

$$d_{C_{12}} = d_1 = g_{C_{12}} \frac{C_{13}}{C_{12}} + p_{C_{12}} \tag{42}$$

$$d_{C_{13}} = d_1 = g_{C_{13}} \frac{C_{load1}}{C_{13}} + p_{C_{13}} \tag{43}$$

And, the total delay of path 2 becomes $D = d_{C_{in}} + d_{C_{11}} + d_{C_{22}}$. If we assume $d_{C_{22}} = d_2$, the delay of path 2 becomes $D = (x_1 x_2 + x_2)d_1 + d_2$. This equation can be rearranged with respect to d_2 as:

$$d_2 = D - (x_1 x_2 + x_2)d_1 \tag{44}$$

With the equal delay model applied to path 2, the following equation is derived.

$$d_{C_{22}} = d_2 = g_{C_{22}} \frac{C_{load2}}{C_{22}} + p_{C_{22}} \tag{45}$$

In path 3, the total delay becomes $D = d_{C_{in}} + d_{C_{31}} + d_{C_{32}}$. With assumption of $d_{C_{31}} = d_{C_{32}} = d_3$, the delay of path 3 becomes $D = x_1 x_2 d_1 + 2d_3$. This equation rearranged with respect to d_3 as:

$$d_3 = \frac{D - x_1 x_2 d_1}{2_1} \tag{46}$$

With the equal delay model applied to path 3, the following equations are derived for each stage.

$$d_{C_{31}} = d_3 = g_{C_{31}} \frac{C_{32}}{C_{31}} + p_{C_{31}} \tag{47}$$

$$d_{C_{32}} = d_3 = g_{C_{32}} \frac{C_{load3}}{C_{32}} + p_{C_{32}} \tag{48}$$

Using the equation (37) through equation (48) and arbitrary x_1 and x_2 value, we can calculate all the capacitance values in Fig. 6.

In Fig. 6, the critical path is assumed to be assigned to the path with two fan-outs in series. The driving gates of the fan-outs are assumed to have a x_1 and x_2 times larger delay respectively than the load gates of the fan-outs at rear. In case of finding x_1 and x_2 parameters that meet the design constraint and minimizing the total capacitances in the circuit, gate sizing for the minimum power dissipation can be obtained.

It is possible to intuitively expand Algorithm 1 to Algorithm 2 which can be applied to the circuit with n fan-out branches. In addition, the equations in Algorithm 2 can be intuitively induced from the topology of the circuit. When a single fan-out branch exists in the circuit, critical stage delay is computed using equation (29), and when double fan-outs exist in series, critical stage delay is computed using equation (39). Therefore, critical stage delay of the circuit (with n fan-outs in series and m stages after the final fan-out node) can be induced from the above two cases as in the following equation (49).

$$d_k = \frac{D}{x_1 x_2 \cdots x_n + x_2 x_3 \cdots x_n + \ldots + x_{n-1} x_n + x_n + m} \tag{49}$$

In a similar manner all other equations can be easily derived from the topology of the circuit.

5. Experiment and Result

In this section we compare the logical effort method with our proposed method in terms of gate sizing obtained by applying them to the two different circuits

At first, we experimented the circuit in Fig. 7 which is composed of inverters with a single fan-out. Secondly, we experimented a 1-bit full adder which is composed of static CMOS gates with many fan-outs inside.

```
Algorithm 2
//MX1 - Set of random x1 values
...
//MXi - Set of random xi values
...
//MXn - Set of random xn values
//MCin - Set of constraint input capacitance values
//old temp - the minimum sum of total capacitances

initialization temp= 0, old temp=∞
for all x1 ∈ MX1 do
 ...
 for all xi ∈ MXi do
  ...
  for all xn ∈ MXn do
   for every multiple paths do
      Calculate delays in all paths
      for every stages of multiple paths do
         Calculate of all capacitance values
       end for
    end for
    Calculate input capacitance value
    if Cin ∈ MCin then
      for every multiple paths do
         for every stages of multiple paths do
            temp = sum of total capacitances
         end for
      end for
    end if
    if temp < old temp then
     old temp = temp
    end if
   end for
  ...
 end for
 ...
end for
```

5.1 An example of multiple paths composed of inverters with single fan-out

Fig. 7 shows a circuit composed of three paths with the input C_{in} and the output C_{load}(=64 (k)). We can assume that path 1 (having four stages) is a critical path and has a 16 (τ) delay. Let each output load have a size of 64 (k) and C_{in} have the value of equal or less than 4 (k).

Table 2 shows the results of gate sizing obtained by applying the algorithm to the circuit of Fig. 7. Table 2 also shows the C_{in} and the sum of gate sizes according to the increment of 0.1 (k) in x value. We can observe that the total sum of gate size is minimized between 0.4 (k) and 0.5 (k) in x value, under the constraint of $C_{in} \leq 4$ (k).

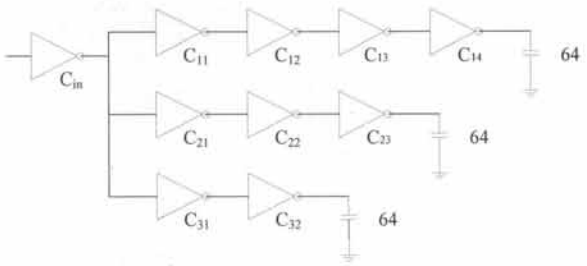

Fig. 7. An example of three paths circuit

Table 3 shows that the total sum of gate size is detailed by the increment of 0.001 (k) in x value, starting from 0.460 (k) to 0.465 (k). According to Table 3, x value (=0.461 (k)) drives the minimum sum of gate sizes and in addition, meets the minimum power dissipation.

Table 4 shows the simulation results of logical effort and our method, respectively. Both methods are applied to the circuit of Fig. 7 under the process of 1.8 (v) and 0.18 (μm) using Hspice. According to the results of simulation, our method is 18 (%) more efficient in power dissipation, compared to that of the logical effort.

Table 2. C_{in} and sum of gate sizes according to the increment of 0.1 (k) in x value

x value	...	0.40	0.50	0.60	0.70	...
Cin	...	5.38	3.50	2.78	2.43	...
sum	...	65.8	66.6	68.7	71.3	...
x value	...	2.50	2.60	2.70	2.80	...
Cin	...	3.77	4.02	4.29	4.59	...
sum	...	158	165	174	182	...

Table 3. C_{in} and sum of gate sizes according to the increment of 0.001 (k) in x value

x value	0.460	0.461	0.462	0.463	0.464	0.465
Cin	4.014	3.998	3.983	3.968	3.953	3.938
sum	66.00	66.01	66.02	66.04	66.05	66.06

Table 4. Results of simulation using Hspice

Technique	Power dissipation (m watts)
logical effort	0.17
Our Method	0.14

5.2 An example of A 1-bit full adder

Fig. 8 shows a 1-bit full adder composed of NOT gates and NAND gates. It can be observed that multiple fan-outs exist in series from input to output. We assume that each output load has a size of 64 (k) and C_{in} has the value of equal or less than 4 (k). If input A in Fig. 8

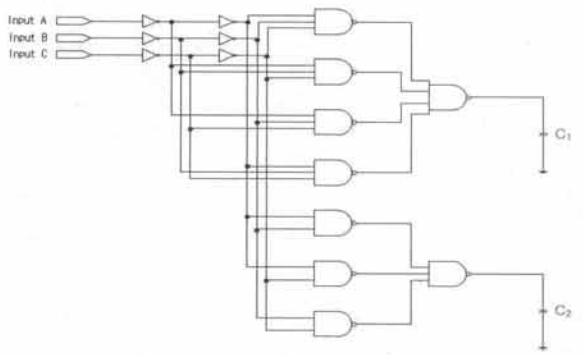

Fig. 8. A 1-bit full adder

is assumed to drive two loads (C_1, C_2) with the other two inputs (input B, input C) having a fixed logic value, then input A goes through 10 gates. We calculated these gate sizes in paths from input A to two loads (C_1, C_2) using logical effort and our methods. Afterwards, we simulated using Hspice under the process of 1.8 (υ) and 0.18 (μm). Table 5 shows the results. According to the results of the simulation, both methods are almost equal in power dissipation, but our method is 52 (%) more efficient in space, compared with that of logical effort. The greater power of driving re-convergent gates used in our method has likely delivered similar total power dissipation for the two methods.

Table 5. Results of simulation using Hspice

Technique	Total size (k)	Power dissipation (m watts)
Logical effort	106	13.9
Our Method	51	13.8

6. Conclusions

We introduced the technique of a multiple-paths gate sizing for optimizing power-delay under a fixed-delay constraint. This technique is based on our previous work and has been extended for multiple logical paths.

For further research, we plan to expand our technique to handle situations where a re-convergent gate exists in the given circuit. Namely, we will develop the method of reducing power dissipation in proportion to size reduction of total gates.

We also envision broadening our research to a point where a known fixed load in a circuit along the path exists and can be measured. As explained in [8], the branching effort does not handle the case where a node has a fixed capacitance value, which is referred to as a side load.

References

[1] Ivan E. Sutherland, and Robert F. Sproull, "logical effort: Designing for Speed on the Back of an Envelope", IEEE Adv. Research in VLSI, MIT Press, 1991.

[2] Ivan Sutherland, Bob Sproull, and David Harris, "logical effort: Designing Fast CMOS Circuits", Morgan Kaufmann Pub., 1999.

[3] Seung Ho Lee and Jong Kwon Chang, "On a Logical Path Design for Optimizing Power-delay under a Fixed-delay Constraint", KIPS, Vol.17-A, No1., 2010.

[4] B. Lasbouygues, S. Engels, R. Wilson, P. Maurine, N. Azemard, and D. Auvergne, "logical effort model extension to propagation delay representation," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol.25, No.9, pp.1677-1684, September, 2006.

[5] Jo Ebergen, Jonathan Gainsley, and Paul Cunningham, "Transistor Sizing: How to Control the Speed and Energy Consumption of a Circuit", Proceedings International Symposium on Advanced Research in Asynchronous Circuits and Systems, IEEE Computer Society Press, 2004.

[6] Chun-Hui Wu, Shun-Hua Lin, Herming Chiueh, "logical effort model extension with temperature and voltage variation", Thermal Investigation of ICs and Systems, 2008.

[7] Haile Yu, Yuk Hei Chan and Leong, P., "FPGA interconnect design using logical effort" Field Programmable Logic and Applications, 2008.

[8] David A. Hodges, Horace G. jackson, and Resve A. Saleh, " Analysis and Design of Digital Integrated Circuits", McGrawHill Pub., 2004.

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