다중칩을 이용한 어레이시스템의 결함허용 설계

김 성 수†

요 약

본 논문에서는 대용량 병렬처리를 위한, 결함허용 다중칩을 이용해서 제조된 어레이시스템에서 여분장치 최적화와 관련된 설계문제를 다룬다. 수율과 신뢰성을 고려한 최적의 비용효과적인 다중칩 설계를 위한 새로운 계량적 방법을 제안하고 결함허용 다중칩의 운영신뢰성에 미치는 잠재여분의 효과를 분석한다. 특히 불완전한 지원회로, 칩조립수율과 어레이위상의 문제들에 대하여 논한다. 광범위에 걸친 분석결과에 따르면 제안한 방법은 수율과 신뢰성을 고려한 대용량 병렬처리 응용분야에 사용되는 다중칩 어레이 설계에 기존방법보다 매우 효율적으로 적용 가능하다.

Fault-Tolerant Design of Array Systems Using Multichip Modules

Sungsoo Kim†

ABSTRACT

This paper addresses some design issues for establishing the optimal number of spare units in array systems manufactured using fault-tolerant multichip modules(MCM's) for massively parallel computing(MPC). We propose a new quantitative approach to an optimal cost-effective MCM system design under yield and reliability constraints. In the proposed approach, we analyze the effect of residual redundancy on operational reliability of fault-tolerant MCM's. In particular, the issues of imperfect support circuitry, chip assembly yield and array topology are investigated. Extensive parametric results for the analysis are provided to show that our scheme can be applied to design arrays using MCM's for MPC applications more efficiently, subject to yield and reliability constraints.

1. Introduction

MCM's consist of complex and dense VLSI devices mounted into packages that allow little physical access to internal nodes. An MCM can be viewed either as a board by its manufacturer, or as a complex system by its user. MCM's provide significant technical and potential economic advantages for high density interconnection and fast VLSI devices. The complexity and costs associated with testing and diagnosis are two of the major obstacles to their extensive use. Unfortunately, today's MCM's are so complex that test methods with 100% fault coverage may not be a vailable [1]. MCM's offer a cost-effective implementation alternative for MPC systems.

In a multiprocessor, an MCM naturally supports a more powerful computing unit with a plurality of microprocessors. The benefits of improved performance at node level (in terms of power consumption and

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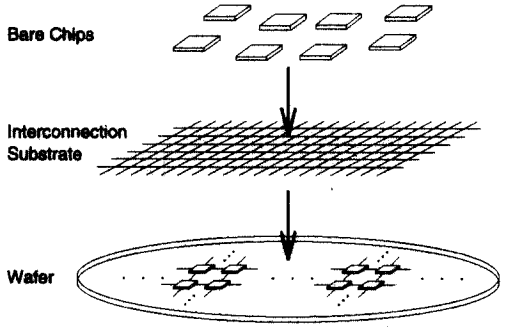
reliability) may have a significant impact at system level in a multinode MPC system. It is also a very realistic alternative as computing node for application to large numerically intensive problem solving. If processor packaging density could be increased then, the number of processor boards and, thereby, production costs for massively parallel computers could be significantly reduced [1].

However MCM's are faced with many problems. Consider yield and reliability for example. One of the keys to economic viability of MCM's is the achievement of high manufacturing yields. Yield losses must be kept very low compared to costs for MCM to remain economically competitive. Even with today's high degree of simulation, test and design aids, systems with millions of gates can have undetected faults which must be repaired [2]. Fault tolerance has been an essential architectural attribute for achieving high reliability in many critical applications of MPC systems due to the increasing number of possible faulty components [3].

In a massively parallel computer with hundreds (or thousands) of processors, the system must have extensive fault-tolerant features to provide service in spite of faults, and system maintenance. It is widely accepted, that it is impossible to rework MCM's in the field. The motivation for introducing fault-tolerance (mainly through redundancy) into these architectures is three-fold : reducing costs through yield enhancement, ensuring on-time delivery and performance improvement (like operational reliability and computational availability).

Since not only defect tolerance before assembly for MCM's is required but also known-good-dies are not universally available, previous methods as [4, 5] are not applicable to MCM's and a different cost-effective design of MCM's has to be adopted to solve these underlying problems. The usage of some form of redundancy has been recently proposed for various MCM designs for MPC [1, 6]. The basic principle of the proposed approaches is to provide some form of redundancy in the system to improve the first-pass-yield of a MPC MCM, i.e. redundant (spare) chips are incorporated into the substrate. One of the first issues with respect to redundancy is to determine how many spares should be included (optimal redundancy). However, the issue of optimal redundancy has not been considered in previous schemes for MCM designs. An optimal cost-effective design is very important for manufacturing fault-tolerant MCM's at competitive costs compared with other approaches [7].

The target system described in this paper, is a two-dimensional array of chips with spare rows and columns for faulty chip replacement. Figure 1 shows the structure of a two-dimensional array of chips in an MCM. Fault tolerance in a processor array is achieved by using a combination of reconfiguration and spare allocation [8, 9]. Reconfiguration is defined as the process of restructuring a faulty system such that the target system can be realized and any faults/defects are eliminated from the system. However, implementation of a particular reconfiguration strategy depends on factors, such as type of circuit under manufacturing, expected reliability, and functionality of the system. In the analytical models considered in this paper, the same redundancy can be used for both yield enhancement and performance improvements. Our analysis points out the possible weakness of the common assumptions of fault-free support circuitry and a perfect assembly yield on an MCM system.



(Fig. 1) Example of the structure of a two-dimensional array in an MCM

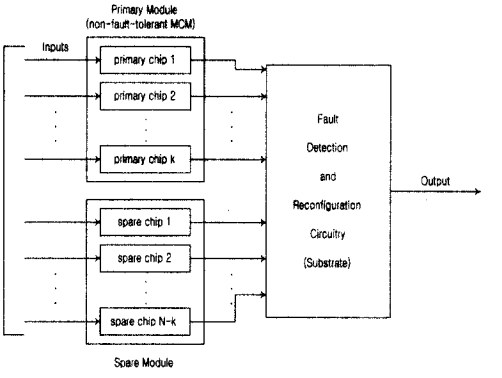
The goal of this paper is to propose efficient quantitative optimal cost-effective design strategies for fault-tolerant arrays in MCM's to maximize cost and delivery benefits. The proposed model takes into account the MCM yield, operational MCM reliability, chip assembly yield, support circuitry failure and array topology to calculate the optimal number of spares for redundancy in a particular system. This paper is organized as follows. In Section 2, we provide the preliminaries which include the modeling assumptions and a brief review of previous work. In Section 3, optimal cost-effective design strategies for fault-tolerant MCM's are discussed. In Section 4, the parametric analysis of the models is presented. Discussion and conclusions are given in Section 5.

2. Review and Preliminaries

For MPC design, time-to-market of MCM's has become crucial. A late design is often obsolete, as cost in a system is of ever increasing concern. While the addition of redundant chips to modules is not practical for all applications, it can be a realistic alternative to extensive chip test or rework [10]. Chip redundancy may be viable for applications in which either space limitation for additional chips is not a major issue, or a large number of identical chips are required. Furthermore, many modules do not require all spare chips to be switched-in during reconfiguration at production-time. This means that the remaining spares can be used for in-service reconfiguration, thus improving reliability and reducing the operating costs [1].

A simple approach to compute the probable first-pass-yield of fault-tolerant MCM's is to use the probability density function (i.e., *pdf*) of a binomial distribution [1, 11]. This method is effective in calculating the yield of a redundant system if no intermediate tests are employed. A limitation of this method is that it can not model intermediate tests. In [6], we have proposed analytical models employing intermediate tests for computing the probable first-pass-yield of fault-tolerant MCM's. In [12], an approach for modeling the economics of manufacturing and test strategies for non-fault-tolerant MCM's at a higher system level, has been presented. The limitation of this method is that both the support circuitry and the assembly were assumed to be perfect. In this paper, we propose three general design strategies to determine the optimal number of spare units for a particular MCM system. This means that our schemes can be applied to all yield models at chip level for fault-tolerant MCM's.

For a system in which k out of n identical, non-repairable units must be operational at a time, the well-known approach for reliability computation also employs the *pdf* of a binomial distribution [10]. This method is effective in calculating the operational reliability of a redundant system provided the support circuitry is fault-free, i.e. only processors can fail. However, a limitation of this method is that it can not incorporate the failure probability of the support circuitry into the reliability expressions-an extremely important aspect in the reliability evaluation of a fault-tolerant system [13]. In this paper, we emphasize the effect of failures in the support circuitry on system reliability and yield, leading to a more realistic and accurate analysis.



(Fig. 2) A fault-tolerant MCM system

In this paper, we model a fault-tolerant MCM system for MPC as a *modified standby sparing system*. The model which we will use for the analysis of fault-tolerant MCM systems, is depicted in Figure 2.

Let N be the number of chips on an MCM and k be the quorum of the required working (fault free) chips. The quorum is the minimum number of required working chips to configure an operational MCM system. In standby sparing [3], one module is operational, while one or more modules are in a standby mode, i.e., spares are employed. Unlike a standby sparing system, our model uses a modified standby sparing in which k chips (i.e., the quorum of the required working (fault-free) chips) are operational and one or more (at most $N-k$) chips are in a standby (spare) mode. Various fault detection schemes can be used to determine when a fault occurs in a chip, and fault location can be used to determine exactly which chip, if any, is faulty [3, 14, 15]. If a fault is detected and located, the faulty chip is removed from on-line (active) operation, and replaced with one of the remaining fault-free spares through the on-circuit reconfiguration circuitry. Reconfiguration can be viewed conceptually as a switching operation, usually implemented through the connectivity of the substrate of the MCM.

As in [1], the following assumptions have been made regarding the yield analysis of our model at production-time : (1) The support circuitry is fault-free. (2) Failure independence is assumed in the chips. (3) Multiple faults are detected and located sequentially, i.e. one after another. (4) After mounting chips, no rework process is employed. (5) The MCM system for MPC is assembled using equally-like chips. This assumption is based on the fact that a closer examination of High Massively Parallel Computer boards usually reveals a regular array of individually packaged, identical chips.

The following assumptions have been made regarding the operational reliability analysis in our model : (1) Unlike most published models, we assume that the support circuitry is not always fault-free during operation, as in [5, 13]. However, note that we assume that the support circuitry is fault-free at production-time, as in [1]. This assumption is based on the fact that larger silicon areas devoted to the support circuitry, increase the hardcore nature and their criticality during operation. (2) Unlike most published models, we assume that several chips can fail simultaneously from a common-cause failure which can occur during operation, as in [16]. However, note that failure independence is assumed in the chips at production-time, as in [1]. (3) Repair of faulty chips in the system has not been taken into account (following the common assumption). This assumption is based on the fact that it is very difficult if not impossible to rework MCM's once they are delivered to the user. (4) Software or operating system faults are not modeled. (5) Only permanent faults are taken into account, thus assuming that the chips will automatically recover from transient faults.

If a die is fault-free, we assume that it is a good die; otherwise, it is assumed to be a bad die. As in [1], we also assume that the known-good-die confidence level (i.e., the probability that a die is fully functional over the specifications and a temperature range) is as follows : $Y_c = q_c \cdot y_b$, where q_c is the quality of an unpackaged chip, and y_b is the die burn-in yield.

Latent defects (usually not screened by a testing procedure) at module level can cause MCM's to fail while installed in a system. Latent defects are physical imperfections that do not affect a circuit functionally, but they may degrade into a faulty condition at a later time. This class of defects is of particular concern because it can result in unexpected failures during operation. Some test methods may cause thermal overstress [12]. For example, thin film surfaces can be sensitive to damage during probing. Also, larger silicon areas devoted to the support circuitry increase the hardcore nature and the criticality of these circuits during operation. As a result, the general assumption of fault-free status for the support circuitry might not be fully valid for MCM's. For evaluating the effects of support circuitry failures on an MCM, we introduce one metric, namely the support circuitry probability of failure, as follows : $S_f(t) = C_s(t) + (1-Y_s \cdot Y_i)$, where $C_s(t)$ is the probability of overstress in the support circuitry, Y_s is the substrate yield, and Y_i is the interconnections yield. Note that $S_f(t)$ is the same as

$C_s(t)$ if both the substrate and the interconnections are assumed to have perfect yields.

As Markov models to predict large and closed form fault-tolerant systems introduce a computational complexity problem due to the large state spaces [11], we will use a combinatorial model to find the reliability and evaluate an optimal redundancy level under some reliability constraints for a particular MCM system. Unlike a previous approach [10], our model incorporates the support circuitry probability of failure into the reliability expression to investigate its effect on the system reliability during operation. This aspect will be dealt in more detail in the next section.

3. Cost-Effective Design Strategies

In this section, three strategies are discussed for designing MCM's [17, 18]. These strategies are substantially different as they try to optimize different figures of merit.

The residual redundancy which can be used for operational reliability improvement, is defined as the redundancy left unused after successfully reconfiguring and eliminating manufacturing defects [5]. Thus, the residual redundancy of a fault-tolerant MCM denoted by s^g (i.e., the number of fault-free spares left unused after fabrication) is given by

$$s^g = N_g - k = \left\lfloor \frac{k}{100}\left(LR - LL - \frac{LR \cdot LL}{100}\right) \right\rfloor \quad (1)$$

where N_g is the number of fault-free chips on a fault-tolerant MCM, LL is the percentage of damaged chips (i.e., the level of first-pass-loss) on an MCM, and LR is the percentage of spare chips (i.e., the level of redundancy) on an MCM.

From (1),

$$LL = 100 - Y_a = \frac{100(N - N_g)}{N} = \frac{100(k \cdot LR - 100 s^g)}{k(100 + LR)} \quad (2)$$

$$LR = \frac{100(N-k)}{k} = \frac{100(100 s^g + k \cdot LL)}{k(100 - LL)} = \frac{100\left|100 s^g + k(100 - Y_a)\right|}{k \cdot Y_a} \quad (3)$$

where the chip assembly yield Y_a is the percentage that a chip has not been damaged during the assembly process.

There are two types of yield : functional yield and parametric yield. Functional yield refers to the successful probability for the MCM to perform the basic functions at completion of manufacturing and is affected by test coverage, process-induced damages, and repairability. Parametric yield refers to the probability of the functional MCM to meet specific performance objectives, such as described in [19]. In this paper, we assume that parametric yield loss is not of primary importance and we consider functional yield only. Apart from optimizing the yield, considerations for an array topology have played a vital role in choosing the appropriate level of redundancy : for example 25% and 12.5% represent a spare row or column for 4×5 and 8×9 two-dimensional array layout of chips, thus conserving the regularity inherent in MPC modules [1].

Reliability is very sensitive to imperfect support circuitry. For short missions requiring an extremely high reliability, system failure (if it occurs) is likely to be caused by the support circuitry rather than a depletion of spares. N Modular redundancy (NMR) is better suited for such applications. Standby sparing is better for long missions in which failure is likely to be caused by depletion of spares [3]. Standby sparing can bring a system back to a full operational capability after the occurrence of a fault, but it requires a momentary disruption in performance while reconfiguration is performed. The total number of chips on an MCM for conserving the regularity inherent in MPC modules with the minimum number of spares varies depending upon an array topology (e.g., with spare rows, spare columns, or spare rows and columns).

3.1 An Optimal Design Strategy for Yield (DFY)

In this case, we assume that the operational reliability constraint (i.e., $R_t(t)$) for an MCM is unknown. The following procedure finds the optimal number of spare chips (denoted by s_y^o) for MPC MCM's, assuming that

the target Y_M (denoted by Y_t) and k are given, where Y_M is the probable first-pass-yield of a fault-tolerant MCM. The algorithm *Design-For-Yield*(Y_t, k, s_y^o) starts by using a yield expression to compute the minimal number of chips on an MCM (denoted by N_m), and then calculates by s_y^o using N_m.

Algorithm 1 : *Design-For-Yield*(Y_t, k, s_y^o)

[Step 1] Find N_m under a yield constraint Y_t using a suitable yield expression for a redundant system (as in [1, 6]). It is assumed that assembly has a perfect yield.

[Step 2] Compute the optimal number of spares s_y^o using the following expressions.

(a) Case 1.1 (denoted by *NCAT*, i.e. with No Considerations for an Array Topology) : If we do not consider an array topology, then by (2)

$$s_y^0 = N - k = \left\lceil N_m - k + \frac{N_m \cdot LL}{100} \right\rceil = \left\lceil \frac{N_m(100+LL)}{100} - k \right\rceil = \left\lceil \frac{N_m(200+Y_a)}{100} - k \right\rceil \quad (4)$$

where since N_m is minimal, N is minimal if Y_a is given.

(b) Case 1.2 (denoted by *CAT*, i.e. with Considerations for an Array Topology) : If we consider an array topology, $s_y^o = N_s - k$, where, N_s = min{ $k = i \cdot n_r,\ k+j \cdot n_c,\ k+i \cdot n_r+j \cdot n_c$} $\geq N$, n_r is the number of chips in a row, n_c is the number of chips in a column, i = 0,1,2, ⋯ and j = 0,1,2, ⋯. N can be computed by using equation (4). Using the above expression, N_s (i.e. the total number of chips on an MCM for conserving the regularity inherent in MPC modules) with the minimum number of spare rows(, columns, or rows and columns), can be obtained efficiently.

We can compute a simple upper bound on the running time of the algorithm *Design-For-Yield*(Y_t, k, s_y^o) as follows. The first step is $O(N_m-k+1)$ time, and the second step is $O(3 \cdot \left\lceil \frac{N-k}{n_r+n_c} \right\rceil)$ time. Thus, the running time is at most $O(N_m+1+3 \cdot \left\lceil \frac{N-k}{n_r+n_c} \right\rceil - k)$.

3.2 An Optimal Design Strategy for Reliability (DFR)

In this case, we assume that the MCM yield constraint (i.e., Y_t) is unknown. The following procedure finds the optimal number of spare chips (denoted by s_r^o) for MPC MCM's, assuming that the target $R_{sys}(t)$ (denoted by $R_t(t)$), k, $R_c(t)$, $S_f(t)$ and the time t are given, where $R_c(t)$ is the reliability of a chip and $R_{sys}(t)$ is the operational system reliability incorporating $S_f(t)$. The algorithm *Design-For-Reliability*($R_t(t)$, k, $R_c(t)$, $S_f(t)$, t, s_r^o) starts by using the operational reliability expression to compute the minimal residual redundancy s^g of a fault-tolerant MCM. Then it calculates the minimal percentage of spare chips LR by using s^g, and finds s_r^o by using LR.

Algorithm 2 : *Design-For-Reliability*($R_t(t)$, k, $R_c(t)$, $S_f(t)$, t, s_r^o)

[Step 1] Find the minimal s^g under a reliability constraint $R_t(t)$ using the following expression.

$$R_t(t) = R_c^k(t) \sum_{i=0}^{s^g} \binom{k}{i} \left[\{1 - S_f(t)\} \{1 - R_c(t)\} \right]^i \quad (5)$$

Note that s^g is determined in terms of $R_c(t)$, $S_f(t)$, k. This expression can be explained as follows. When the system goes into operation, at most s_g chips are in a standby (spare) mode to improve its operational reliability by handling only operational faults. In expression (5) we incorporate the effect of failures in the support circuitry on system reliability by employing the term $\{1-S_f(t)\}^i$.

[Step 2] Compute the minimal LR using equation (3) in which s^g is minimal.

[Step 3] Compute the optimal number of spares s_r^o

using the following expressions.

(a) Case 2.1 (denoted by *NCAT*) : If we do not consider an array topology,

$$s_r^0 = N - k = \left\lceil \frac{LR}{100} \cdot k \right\rceil \quad (6)$$

where N is minimal if LR is minimal.

(b) Case 2.2 (denoted by *CAT*) : If we consider an array topology, $s_r^o = N_s - k$, where $N_s = \min\{k+i \cdot n_r, k+j \cdot n_c, k+i \cdot n_r + j \cdot n_c\} \geq N$, n_r is the number of chips in a row, n_c is the number of chips in a column, $i = 0,1,2,\cdots$ and $j = 0,1,2,\cdots$. N can be computedby using equation (6).

We can compute a simple upper bound on the running time of the algorithm *Design-For-Reliability*($R_t(t)$, k, $R_c(t)$, $S_f(t)$, t, s_r^o)as follows. The first step costs$O(s^g+1)$time, the second step costs $O(1)$ time, and the third step costs $O(3 \cdot \left\lceil \frac{N-k}{n_r+n_c} \right\rceil)$ time. Thus, the running time is at most $O(s^g+2+3 \cdot \left\lceil \frac{N-k}{n_r+n_c} \right\rceil)$.

3.3 An Optimal Design Strategy for Yield and Reliability (DFYR)

If the reliability constraint $R_t(t)$ is not available, this is the same scenario as the DFY Strategy; if the yield constraint Y_t is not available, this corresponds to the DFR Strategy. The following four procedures subject to $S_f(t)$ and Y_a, find the optimal number of spare chips (denoted by s^o) for MPC MCM's, assuming that Y_t, $R_t(t)$, k, $R_c(t)$ and t are given.

Case 3.1 : The support circuitry probability of failure $S_f(t)$ is the only unknown.

Algorithm 3.1 : Design-For-Yield-And-Reliability1 (Y_t, $R_t(t)$, k, $R_c(t)$, $S_f(t)$, t, s_{lo}^o)

[Step 1] Compute s_y^o by using *Algorithm 1 : Design-For-Yield*(Y_t, k, s_y^o).

[Step 2] If the support circuitry is fault-free (i.e., $S_f(t) = 0$), compute s_r^o by using *Algorithm 2 : Design-For-Reliability*($R_t(t)$, k, $R_c(t)$, $S_f(t)$, t, s_r^o).

[Step 3] Compute s_{lo}^o (i.e. a lower bound of s^o) as follows.

$$s^o \geq s_{lo}^o = s_y^o, \text{ if } s_y^o \geq s_r^o$$
$$s^o \geq s_{lo}^o = s_r^o, \text{ otherwise.} \quad (7)$$

Case 3.2 : The chip assembly yield Y_a is the only unknown.

Algorithm 3.2 : *Design-For-Yield-And-Reliability2*(Y_t, $R_t(t)$, k, $R_c(t)$, $S_f(t)$, t, s_{lo}^o)

[Step 1] If the assembly has a perfect yield (i.e., Y_a=100%), compute s_y^o by using *Algorithm 1 : Design-For-Yield*(Y_t, k, s_y^o).

[Step 2] If the assembly has a perfect yield (i.e., Y_a=100%), compute s_r^o by using *Algorithm 2 : Design-For-Reliability*($R_t(t)$, k, $R_c(t)$, $S_f(t)$, t, s_r^o).

[Step 3] Compute s_{lo}^o by using equation (7).

Case 3.3 : Both $S_f(t)$ and Y_a are unknown.

Algorithm 3.3 : *Design-For-Yield-And-Reliability3* (Y_t, $R_t(t)$, k, $R_c(t)$, $S_f(t)$, t, s_{lo}^o)

[Step 1] If the assembly has a perfect yield (i.e., Y_a=100%), compute s_y^o by using *Algorithm 1 : Design-For-Yield*(Y_t, k, s_y^o).

[Step 2] If the support circuitry is fault-free and the assembly has a perfect yield (i.e., $S_f(t)$=0 and Y_a=100%), compute s_r^o by using *Algorithm 2 : Design-For-Reliability*($R_t(t)$, k, $R_c(t)$, $S_f(t)$, t, s_r^o).

[Step 3] Compute s_{lo}^o by using equation (7).

Case 3.4 : Both $S_f(t)$ and Y_a are known.

Algorithm 3.4 : *Design-For-Yield-And-Reliability4* $(Y_t, R_t(t), k, R_c(t), S_f(t), t, s^o)$

[Step 1] Compute s_y^o by using *Algorithm 1* : *Design-For-Yield*(Y_t, k, s_y^o).

[Step 2] Compute s_r^o by using *Algorithm 2* : *Design-For-Reliability*$(R_t(t), k, R_c(t), S_f(t), t, s_r^o)$.

[Step 3] Compute the optimal number of spares s^o as follows.

$$s^o = s_y^o, \text{ if } s_y^o \geq s_r^o$$
$$s^o = s_r^o, \text{ otherwise.} \quad (8)$$

Note that s^o for the MPC MCM system can be determined only provided both $S_f(t)$ and Y_a are also known. Otherwise, only s_{lo}^o can be computed under the given assumptions.

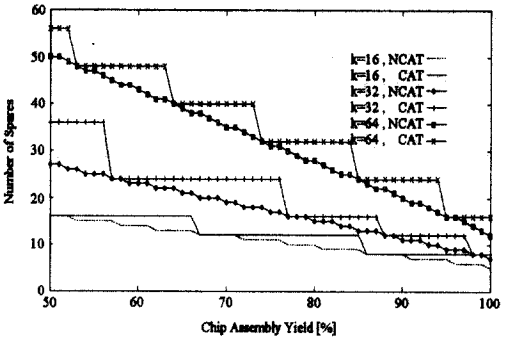
4. Parametric Analysis

In this section, we will study the effect of the above three design strategies for cost-effectiveness and on-time delivery of fault-tolerant MCM's for MPC. In particular, the issues of imperfect support circuitry, chip assembly yield and array topology are investigated.

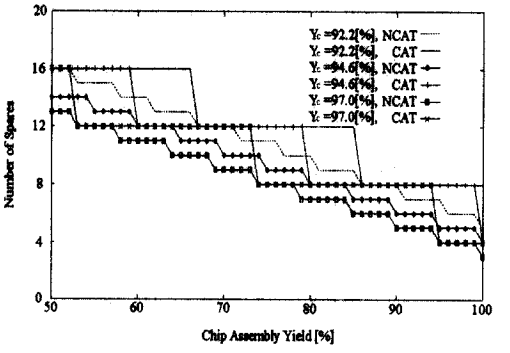
Typical values for die quality and burn-in yield depend on the complexity of the chip itself. In this analysis, we use a known-good-die confidence level in the range of $92.2\% < Y_c < 97.0\%$, i.e., the same range as assumed in [1, 6]. For simplicity, it is also assumed that the chips in operation follow an exponential failure law with a same constant failure rate (given by λ). To assure that MCM systems meet the highest quality and reliability objectives and yet remain competitively priced, the data used in the following illustrations are : $Y_t = 0.99$, $R_t(t_i) = 0.999$, $R_t(t_i) = = e^{-0.001} = 0.999$, and $\lambda = 7.69 \times 10^{-8}$ [failures/hour] $= 6.74 \times 10^{-4}$ [failures/year] (i.e. the same value of as in [20]) where $t_i = 13000$ [hours] $= 1.484$ [years] for satisfying both $R_t(t_i) = 0.999$ and $R_c(t_i) = 0.999$.

In Figure 3, we show the effects of chip assembly yield and array topology on an optimal redundancy under the DFY Strategy assuming $Y_c = 92.2\%$ for systems requiring 16, 32 and 64 working dies. In Figures 4 and 5, we show the impact of chip assembly yield and array topology on an optimal redundancy under the DFY Strategy assuming different known-good-die confidence levels for a system requiring 16 and 64 working dies, respectively. As expected, all examples demonstrate that for a given k the required number of spares decreases as the chip assembly yield (and/or the known-good-die confidence level) is (are) increased. Figure 6 demonstrates the residual redundancy effect on operational MCM reliability under the DFY Strategy by assuming a perfect assembly yield and different support circuitry probabilities of failure for systems requiring 16, 32 and 64 working dies. This figure shows that the larger the number of spares (and/or the smaller the support circuitry probability of failure), the higher the operational reliability of the system; however the most pronounced improvement occurs by providing only one spare.

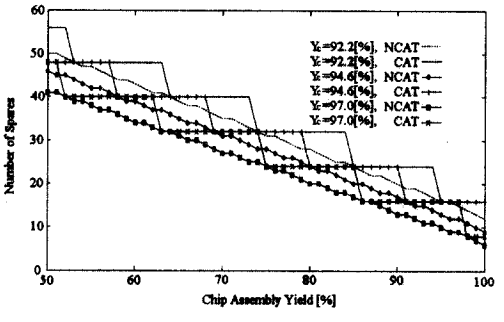
In Figure 7, we show the effects of chip assembly yield and array topology on an optimal redundancy under the DFR Strategy by assuming $Y_c = 92.2\%$ for systems requiring 16, 32 and 64 working dies. In Figures 8 and 9, we show the impacts of chip assembly yield and array topology on an optimal redundancy under the DFR Strategy for different known-good-die confidence levels in systems requiring 16 and 64 working dies, respectively. In Figures 7, 8 and 9, it is assumed that $S_f(t_i) = 0.01$. As expected, the known-good-die confidence level in these Figures shows no effect on the optimal redundancy under the DFR Strategy, whereas the number of spares also decreases as the chip assembly yield is increased. Figure 10 demonstrates the effect of chip redundancy on MCM yield under the DFR Strategy for a perfect assembly yield and different known-good-die confidence levels in systems requiring 16, 32 and 64 working dies. This figure shows that the larger the number of spares (and/or



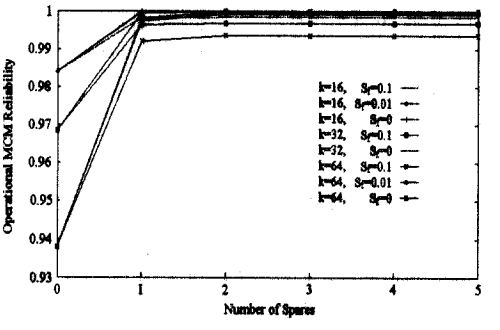
(Fig. 3) Chip assmebly yield effect on an optimal redundancy under the DFY strategy (Yc=92.2[%])



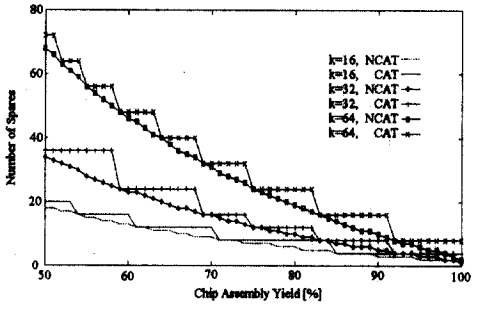
(Fig. 4) Chip assmebly yield effect on an optimal redundancy under the DFY strategy (k=16)



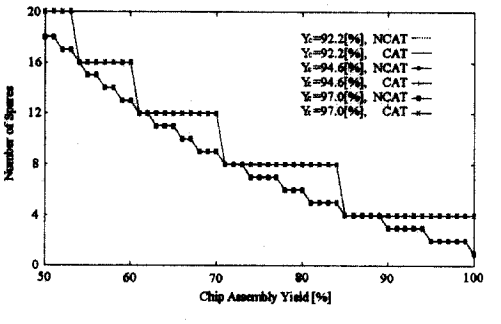
(Fig. 5) Chip assembly yield effect on an optimal redundancy under the DFY strategy (k=64)



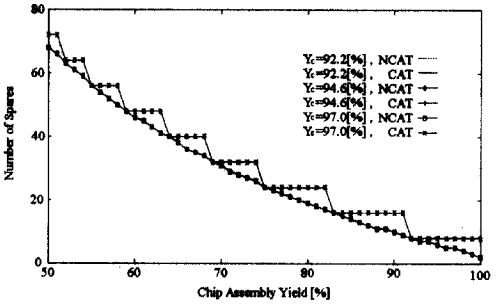
(Fig. 6) Residual redundancy effect on operational MCM reliability (DFY, Y_s=100[%], $\lambda = 7.69\times10^{-9}$[failures/hour])



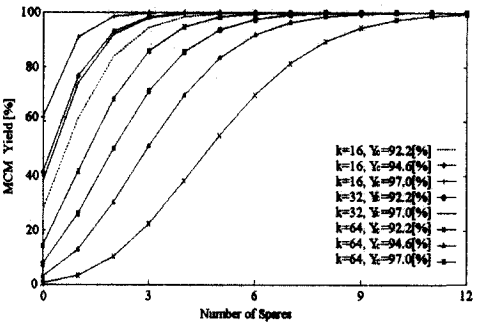
(Fig. 7) Chip assembly yield and optimal redundancy under the DFR strategy (S_f=0.01, Y_c=92.2[%])



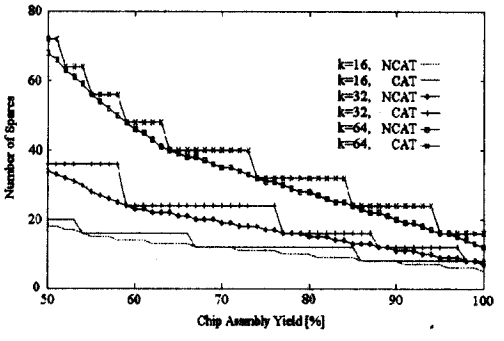
(Fig. 8) Chip assembly yield and optimal redundancy under the DFR strategy (S_f=0.01, k=16)



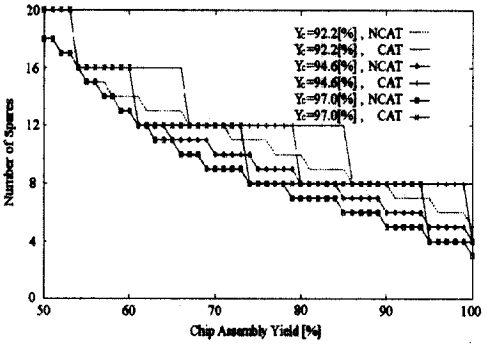
(Fig. 9) Chip assembly yield and optimal redundancy under the DFR strategy
(S_f=0.01, k=64)



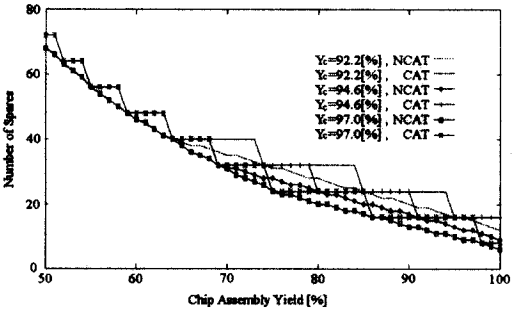
(Fig. 10) Effect of chip redundancy on MCM yield
(DFR, Y_a=100[%])



(Fig. 11) Chip assembly yield effect on optimal redundancy under the DFYR strategy
(S_f=0.01, Y_c=92.2[%])



(Fig. 12) Chip assembly yield effect on optimal redundancy under the DFYR strategy
(S_f=0.01, k=16)



(Fig. 13) Chip assembly yield effect on optimal redundancy under the DFYR strategy
(S_f=0.01, k=64)

the larger the known-good-die confidence level), the higher the probable first-pass-yield of an MCM.

In Figure 11, we show the effects of chip assembly yield and array topology on the optimal redundancy under the DFYR Strategy assuming Y_c=92.2% for systems requiring 16, 32 and 64 working dies. In Figures 12 and 13, we show the impact of chip assembly yield and array topology on the optimal redundancy under the DFYR Strategy assuming different known-good-die confidence levels for a system requiring 16 and 64 working dies, respectively. In Figures 11, 12 and 13, it is also assumed that $S_i(t_i)$=0.01. As expected, all examples clearly demonstrate that the number of required spares decreases, as the chip assembly yield (and/or the known-good-die confidence level) is (are) increased.

By comparing Figures 3, 7 and 11, we note that the DFY Strategy may provide a better figure of merit than other strategies in a practical scenario, provided the chip assembly yield is below a certain value. For high values of chip assembly yield, the DFR Strategy is better. These observations are based on the fact that if the reliability constraint $R_t(t)$ is not available, the DFYR Strategy provides the same scenario as the DFY Strategy; if the yield constraint Y_t is not available, the DFYR Strategy corresponds to the DFR Strategy. From the analysis of the results, it is also shown that although an idealistic assumption with certain possible limitations (such as fault-free support circuitry, a perfect assembly yield and no array topology considerations) in the literature [1, 6, 12] can simplify the theoretical analyses, the obtained results may prove to be too optimistic and misleading for MCM technology.

〈Table 1〉 Comparison between the proposed optimal design strategies

Design Strategy	MCM Yield Constraint Y_t	MCM Reliability Constraint $R_t(t)$	Chip Assembly Yield
DFY strategy	known	unknown	good for low values
DFR strategy	unknown	known	good for high values
DFYR strategy	known	known	good for middle values

5. Discussion and Conclusions

It has been widely recognized that the supply of known-good-die can only provide a partial solution to the cost and delivery problems of MCM systems; in order to solve the underlying manufacturing and production problems, a different approach must be adopted. The use of an extensive chip test or rework processes may not be practical for all applications, therefore an alternative solution is to add redundant chips to modules. An optimal cost-effective design is very important to manufacture fault-tolerant MCM's at a competitive cost compared with alternative technologies and approaches [1, 10].

This paper has proposed new optimal design strategies for cost-effectiveness and on-time delivery of fault-tolerant MCM's for MPC. The objective is to minimize the number of spare units in a system, while improving the yield and reliability of MCM's. Comparison between the proposed design strategies is shown in Table 1.

It may be noted that in today's MCM technology, although the general assumptions of an ideal support circuit, perfect assembly yield and no system considerations, can simplify the analysis, the results so obtained are not realistic. In addition, the analysis of the effect of residual redundancy on operational reliability of fault-tolerant MCM's has been presented. Our method allows an accelerated search for the optimal number of spares as predicted by the analytical models, thereby achieving significant time gains for establishing an optimal level of redundancy. Also, this technique enables to predict accurate field service via reliability modeling as well as managing the system yield. From analyzing the results, we note that the number of required spares decreases, as the chip assembly yield (and/or the known-good-die confidence level) is (are) increased. We also note that

the larger the number of spares (and/or the smaller the support circuitry probability of failure), the higher the operational reliability of the system. Extensive parametric analysis results have shown that our approach can be applied to the designs for yield and reliability of MCM systems for MPC more efficiently than previously. In addition, our method can be easily implemented as an automatic tool for establishing the optimal redundancy of fault-tolerant MCM's for MPC.

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